Refine Search

Search Results -

Terms	Documents
"helper flip flop" or "helper flip-flop"	69

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 06, 2005 Printable Copy Create Case

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	"helper flip flop" or "helper flip-flop"	69	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
"helper flip flop" or "helper flip-flop"	7

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 06, 2005 Printable Copy Create Case

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	"helper flip flop" or "helper flip-flop"	69	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

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Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 06, 2005 Printable Copy Create Case

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L2	"helper flip flop" or "helper flip-flop"	
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L1	"helper flip flop" or "helper flip-flop"	6

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L3	38

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 06, 2005 Printable Copy Create Case

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	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L1	"helper flip flop" or "helper flip-flop"	6

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L4 and (bus near5 width)	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 06, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count
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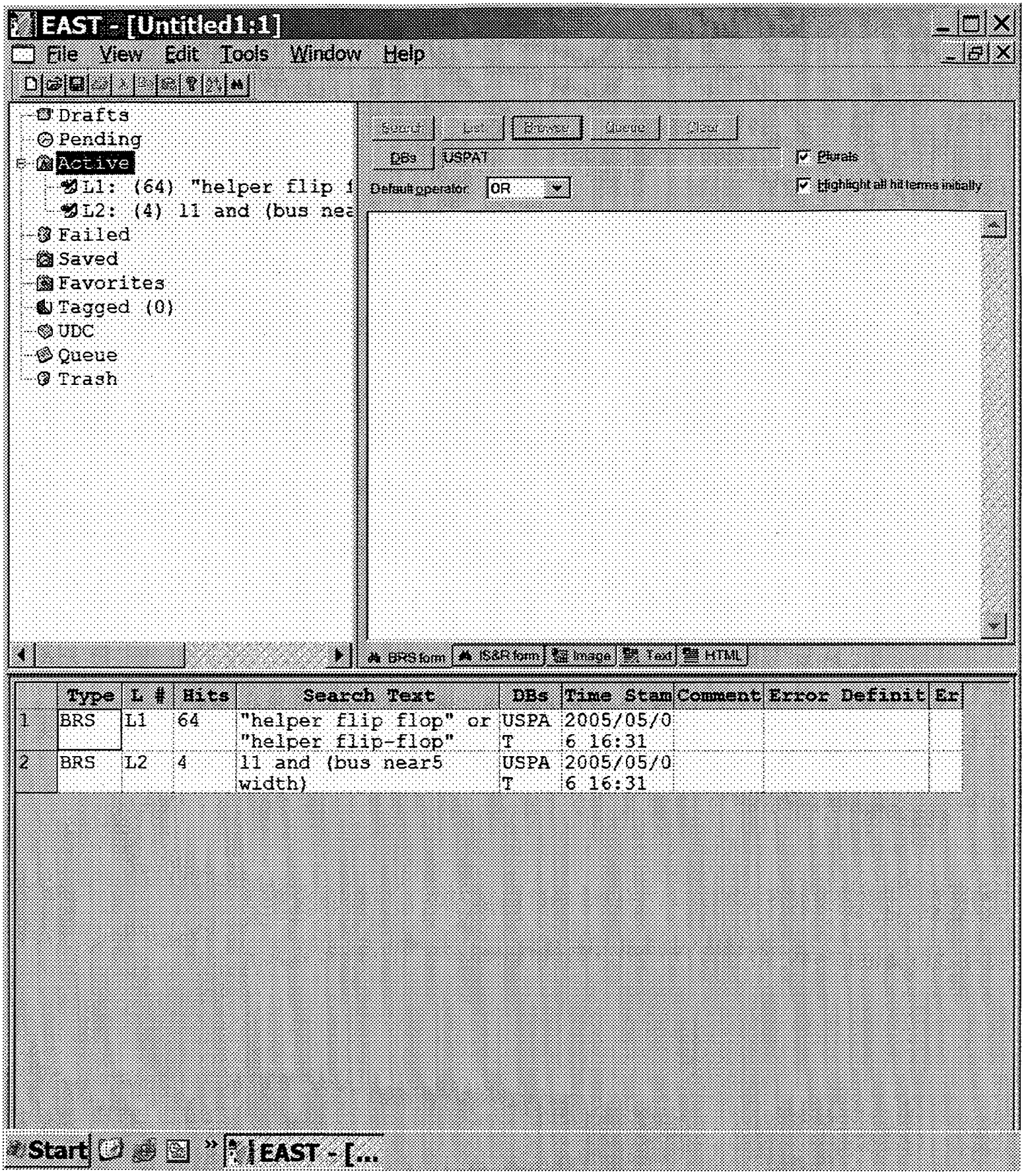
L1	"helper flip flop" or "helper flip-flop"	6

END OF SEARCH HISTORY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File View Edit Tools Window Help
Drafts
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OR
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1 BRS L1 64 "helper flip flop" or "helper flip-flop" USPAT 2005/05/06 16:31
2 BRS L2 4 l1 and (bus near5 width) USPAT 2005/05/06 16:31
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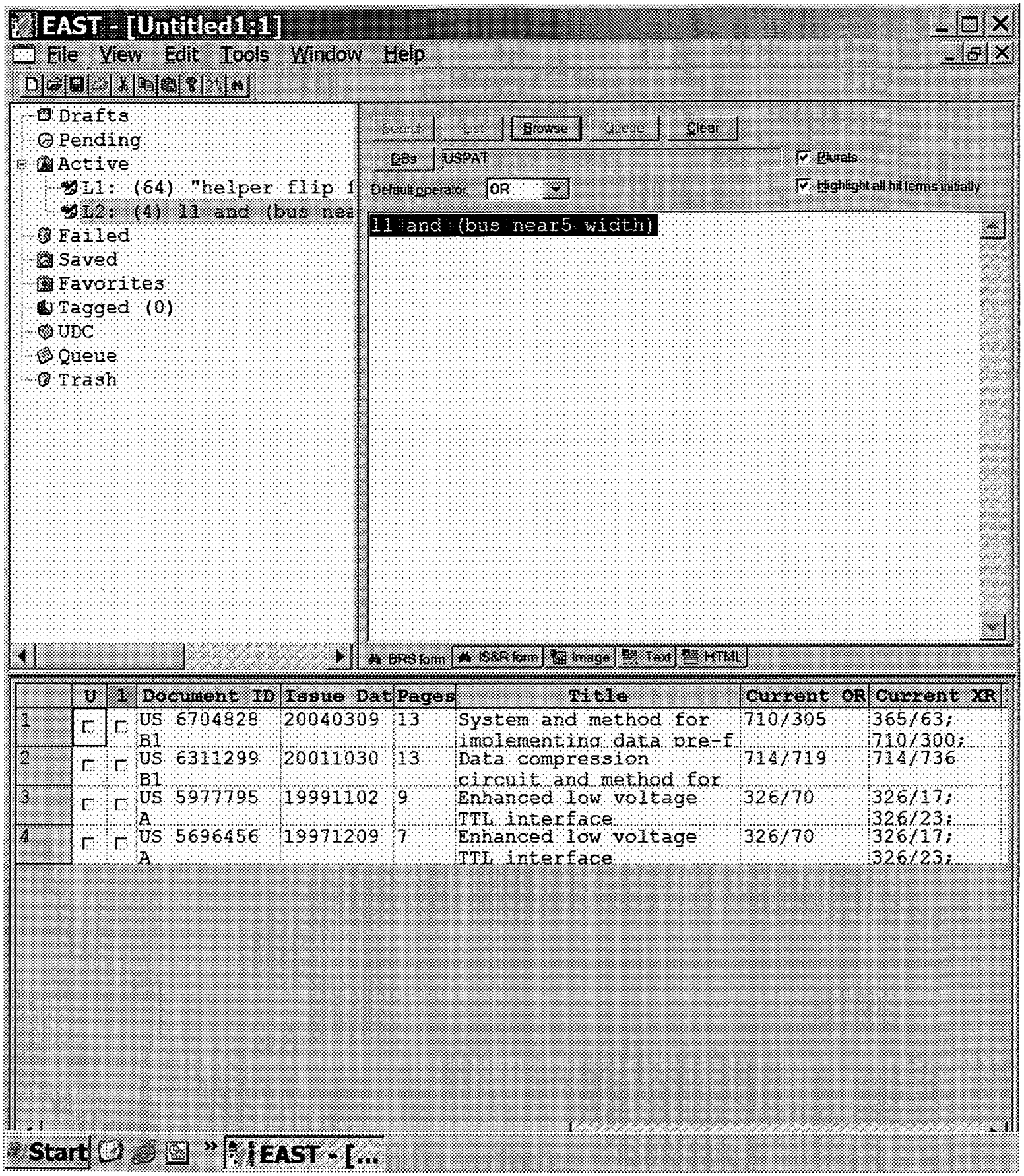
EAST - [Untitled1:1]
File View Edit Tools Window Help
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Browse
Queue
Clear
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USPAT
Plurals
Highlight all hit terms initially
Default operator:
OR
l1 and (bus near5 width)
BRS form
IS&R form
Image
Text
HTML
U
L
Document ID
Issue Dat
Pages
Title
Current OR
Current XR
1
US 6704828 B1
20040309
13
System and method for implementing data pre-f
710/305
365/63; 710/300;
2
US 6311299 B1
20011030
13
Data compression circuit and method for
714/719
714/736
3
US 5977795 A
19991102
9
Enhanced low voltage TTL interface
326/70
326/17; 326/23;
4
US 5696456 A
19971209
7
Enhanced low voltage TTL interface
326/70
326/17; 326/23;
Start
EAST - [...

Results for "(helper flip flop<in>metadata) <and> (bus width<in>metadata)"

Your search matched 0 of 1154623 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» View Session History

» New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(helper flip flop<in>metadata) <and> (bus width<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

Results for "(flip flop<in>metadata) <and> (bus width<in>metadata)" e-mail printer friendly

Your search matched 1 of 1154623 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» View Session History

» New Search

Modify Search

(flip flop<in>metadata) <and> (bus width<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **An intelligent, self-deducing graphical register transfer interface based on a distributed constraint logic computation**
Jennings, G.;
Design Automation Conference, 1995. Proceedings of the ASP-DAC '95/CHDL '95/VLSI '95., IFIP International Conference on Hardware Description Languages; IFIP International Conference on Very Large Scale Integration., Asian and South Pacific
29 Aug.-1 Sept. 1995 Page(s):581 - 586
AbstractPlus | Full Text: PDF(628 KB) IEEE CNF

An intelligent, self-deducing graphical register transfer interface based on a distributed constraint logic computation

Jennings, G.
Div. of Comput. Eng., Lulea Inst. of Technol., Sweden;

This paper appears in: **Design Automation Conference, 1995. Proceedings of the ASP-DAC '95/CHDL '95/VLSI '95., IFIP International Conference on Hardware Description Languages; IFIP International Conference on Very Large Scale Integration., Asian and South Pacific**
Publication Date: 29 Aug.-1 Sept. 1995
On page(s): 581 - 586
Meeting Date: 08/29/1995 - 09/01/1995
Location: Chiba
INSPEC Accession Number:5224562
DOI: 10.1109/ASPDAC.1995.486373
Posted online: 2002-08-06 19:53:08.0

Abstract
We present a graphical capture tool for register transfer level modeling which is capable of deducing **bus widths** and other such undeclared circuit parameters with minimal user intervention. Known design parameters are self-propagated over the entire circuit, and can lead for example to all undeclared **bus widths** becoming automatically defined. This frees the designer from explicitly declaring those circuit features which the tool can deduce. Furthermore this provides fully generic n-bit m-input components, such as "wide **flip-flops**" having uncommitted width, at that point in the design cycle when such constructs are most needed. The novel use of constraints within individual model elements, together with a distributed constraint logic computation, provides the deductive mechanism. We describe the facility and examine its performance on a number of test cases

Index Terms
Inspec
Controlled Indexing
constraint handling graphical user interfaces logic CAD logic design

Non-controlled Indexing
bus widths constraint logic computation deductive mechanism graphical capture tool register transfer interface register transfer level modeling uncommitted width wide **flip-flops**
Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

View Search Results

L5: Entry 1 of 2 File: PGPB Sep 9, 2004

PGPUB-DOCUMENT-NUMBER: 20040177208
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040177208 A1

TITLE: Reduced data line pre-fetch scheme

PUBLICATION-DATE: September 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Merritt, Todd A.	Boise	ID	US	
Morgan, Donald M.	Meridian	ID	US	

APPL-NO: 10/ 773074 [PALM]
DATE FILED: February 5, 2004

RELATED-US-APPL-DATA:
Application 10/773074 is a division-of US application 09/652390, filed August 31, 2000, US Patent No. 6704828

INT-CL: [07] G06 F 13/14

US-CL-PUBLISHED: 710/305
US-CL-CURRENT: 710/305

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A data amplifier configured to allow for fewer data lines and/or increased processing speeds. Specifically, multiple helper flip-flops are used to prefetch data in a data amplifier. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines. Alternatively, the number of data lines can be maintained and faster bus processing speeds may be realized.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a divisional of U.S. application Ser. No. 09/652,390, filed on Aug. 31, 2000.

Generate Collection Print

L5: Entry 2 of 2 File: USPT Mar 9, 2004

US-PAT-NO: 6704828
DOCUMENT-IDENTIFIER: US 6704828 B1

TITLE: System and method for implementing data pre-fetch having reduced data lines and/or higher data rates

DATE-ISSUED: March 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Merritt; Todd A.	Boise	ID		
Morgan; Donald M.	Meridian	ID		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 09/ 652390 [PALM]
DATE FILED: August 31, 2000

INT-CL: [07] G06 F 13/38, G06 F 13/40, G06 F 12/00, G11 C 5/06

US-CL-ISSUED: 710/305; 710/300, 711/100, 712/33, 365/63
US-CL-CURRENT: 710/305; 365/63, 710/300, 711/100, 712/33

FIELD-OF-SEARCH: 710/100, 710/300, 710/305, 365/63, 365/189.01, 365/230.01, 365/230.08, 365/205, 330/3, 713/501, 711/100, 711/103, 712/33, 327/266, 327/287

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4014006	March 1977	Sorensen et al.	
☐	4947373	August 1990	Yamaguchi et al.	
☐	5006980	April 1991	Sanders et al.	
☐	5463582	October 1995	Kobayashi et al.	
☐	6026050	February 2000	Baker et al.	
☐	6166942	December 2000	Vo et al.	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Fletcher Yoder

ABSTRACT:

A method and apparatus for reducing the number of data read lines needed in a memory device. Specifically, multiple helper flip-flops are used to prefetch data in a memory device. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines.

18 Claims, 7 Drawing figures

Previous Doc Next Doc Go to Doc#

US006704828B1

(12) **United States Patent**
Merritt et al.

(10) **Patent No.: US 6,704,828 B1**
(45) **Date of Patent: Mar. 9, 2004**

(54) **SYSTEM AND METHOD FOR IMPLEMENTING DATA PRE-FETCH HAVING REDUCED DATA LINES AND/OR HIGHER DATA RATES**

(75) Inventors: Todd A. Merritt, Boise, ID (US); Donald M. Morgan, Meridian, ID (US)

(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 524 days.

(21) Appl. No.: 09/652,390

(22) Filed: Aug. 31, 2000

(51) Int. Cl.[7] G06F 13/38; G06F 13/40; G06F 12/00; G11C 5/06

(52) U.S. Cl. 710/305; 710/300; 711/100; 712/33; 365/63

(58) Field of Search 710/100, 300, 710/305; 365/63, 189.01, 230.01, 230.08, 205; 330/3; 713/501; 711/100, 103; 712/33; 327/266, 287

(56) References Cited

U.S. PATENT DOCUMENTS

4,014,005 A * 3/1977 Sorensen et al.
4,947,373 A * 8/1990 Yamaguchi et al.
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5,463,582 A * 10/1995 Kobayashi et al.
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6,166,942 A * 12/2000 Vo et al.

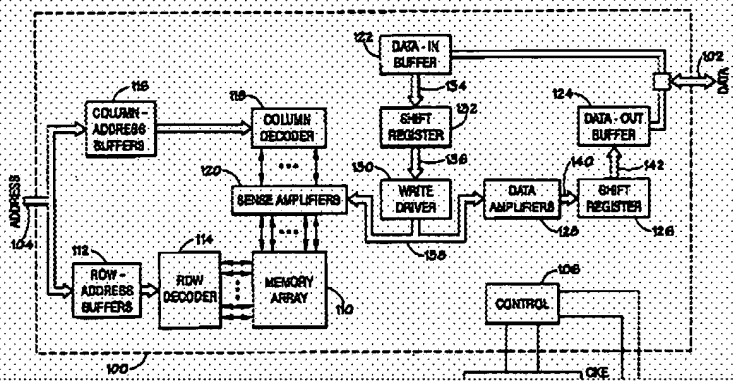
* cited by examiner

Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Fletcher Yoder

(57) **ABSTRACT**

A method and apparatus for reducing the number of data read lines needed in a memory device. Specifically, multiple helper flip-flops are used to prefetch data in a memory device. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines.

18 Claims, 7 Drawing Sheets



US006311299B1

(12) **United States Patent**
Bunker

(10) **Patent No.: US 6,311,299 B1**
(45) **Date of Patent: Oct. 30, 2001**

(54) **DATA COMPRESSION CIRCUIT AND METHOD FOR TESTING EMBEDDED MEMORY DEVICES**

(75) Inventor: Layne G. Bunker, Boise, ID (US)

(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/260,989

(22) Filed: Mar. 1, 1999

(51) Int. Cl.[7] G11C 29/00; G01R 31/28; G06F 11/00

(52) U.S. Cl. 714/719; 714/736

(58) Field of Search 714/3, 5, 6, 9, 714/718, 719

(56) **References Cited**

U.S. PATENT DOCUMENTS

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6,163,875	*	12/2000	Suzuki	716/4

* cited by examiner

Primary Examiner—Albert Decady
Assistant Examiner—Joseph D. Torres

(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

A test circuit enables a memory tester to test for defective memory cells in a memory portion of an Embedded DRAM or other memory device having a relatively wide internal data path. The Embedded DRAM includes a memory having an array of memory cells, the memory being coupled to a logic circuit. The test circuit includes at least one external terminal and a plurality of data masking circuits. Each data masking circuit is coupled to a respective one of the arrays and transfers data signals to and from addressed memory cells in the array. The data signals are selectively masked responsive to a data masking signal. A plurality of data compression circuits each is coupled to a respective data masking circuit to receive a respective data signal. Each data compression circuit compares each of the data signals applied on its respective inputs to an expected value and generates an active error signal on a respective external terminal responsive to any of the applied data signals not having the expected value. When the test mode signal goes active, a test control circuit applies addressed data to the data masking circuits. The control circuit initially disables the data masking signals so the addressed data is not masked and controls the data compression circuits to generate the respective error signals responsive to the applied data. When at least one the error signals goes active, the test control signal goes active causing the test control circuit to control the data masking signals to sequentially mask each data signal applied to the data masking circuit that generated the active error signal to enable an external tester to detect a defective memory cell from the error signals.

33 Claims, 3 Drawing Sheets